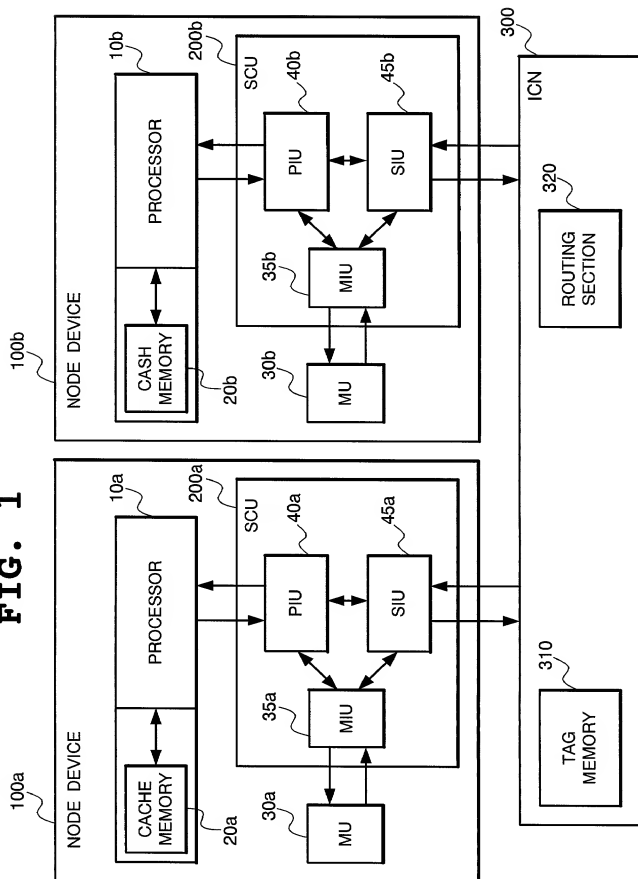


**FIG. 1**

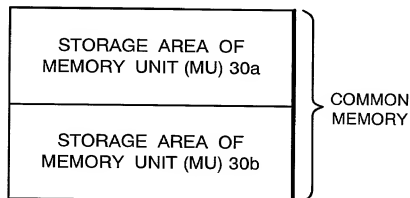
**FIG. 2**

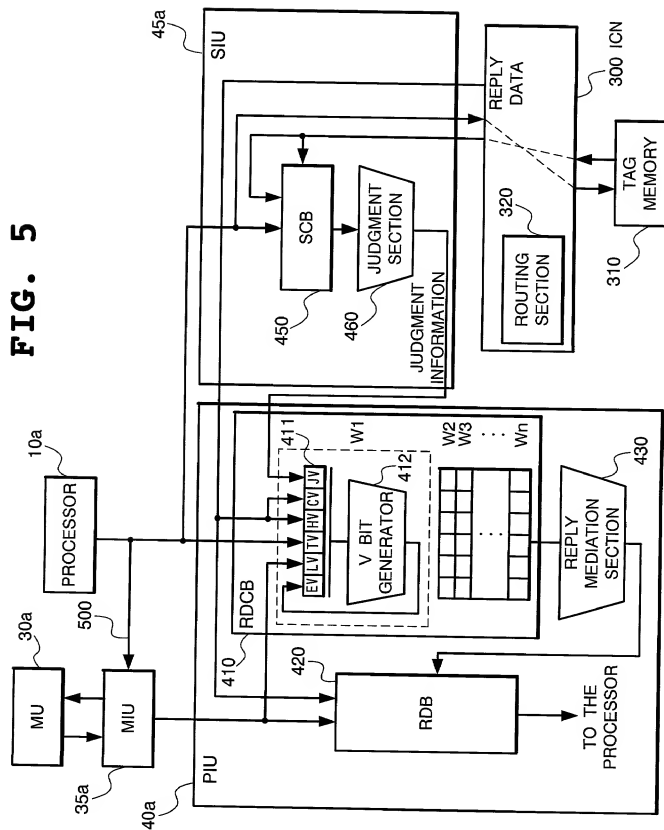
TAG INFORMATION

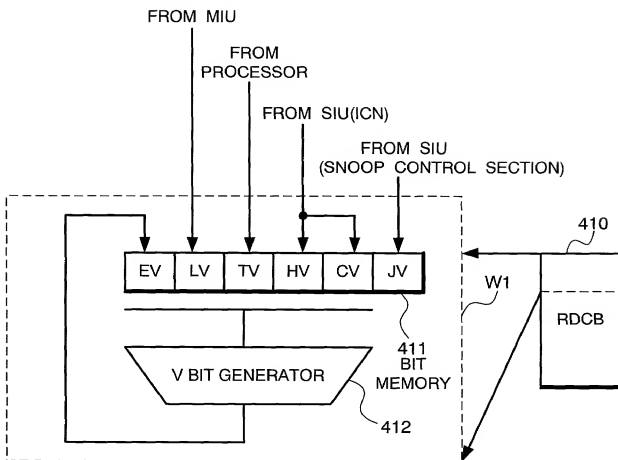
BLOCK NUMBER	STATUS INFORMATION	NODE DEVICE NUMBER
a	U	
b	S	1, 2
⋮	⋮	⋮
n	P	2

**FIG. 3**

STATUS INFORMATION	CACHE STATUS
U	CACHE DATA IS NOT FOUND IN ANY OF THE NODE DEVICES
S	DATA IN THE CACHE IS IDENTICAL TO THE DATA IN THE MEMORY UNIT AND THE SAME CACHE DATA IS FOUND IN SEVERAL NODE DEVICES
P	CACHE DATA IS FOUND IN ONE NODE DEVICE ONLY

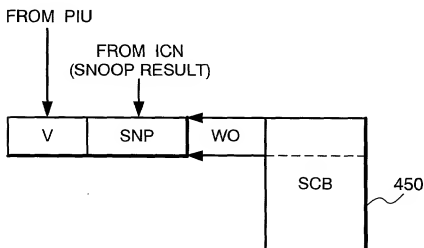
**FIG. 4**

**FIG. 5**

**FIG. 6**

**FIG. 7**

EV	REPRESENTATIVE BIT OF ENTRY SHOWING THAT THE CONDITIONS TO SEND THE REPLY DATA TO THE PROCESSOR ARE ESTABLISHED
LV	BIT SHOWING THAT THE REPLY DATA BY THE SPECULATIVE READ PATH HAS BEEN RETURNED FROM THE LOCAL MEMORY
TV	BIT SHOWING THAT A READ TYPE TRANSACTION HAS BEEN RECEIVED FROM THE PROCESSOR AND ISSUED TO THE SIU / MIU
HV	BIT SHOWING THAT THE REPLY DATA HAS BEEN RETURNED FROM THE MEMORY UNIT (MU) MOUNTED ON THE OTHER NODE
CV	BIT SHOWING THAT MODIFY DATA HELD IN THE CACHE OF THE REMOTE NODE HAS BEEN RETURNED
JV	BIT SHOWING THE SNOOP RESULT

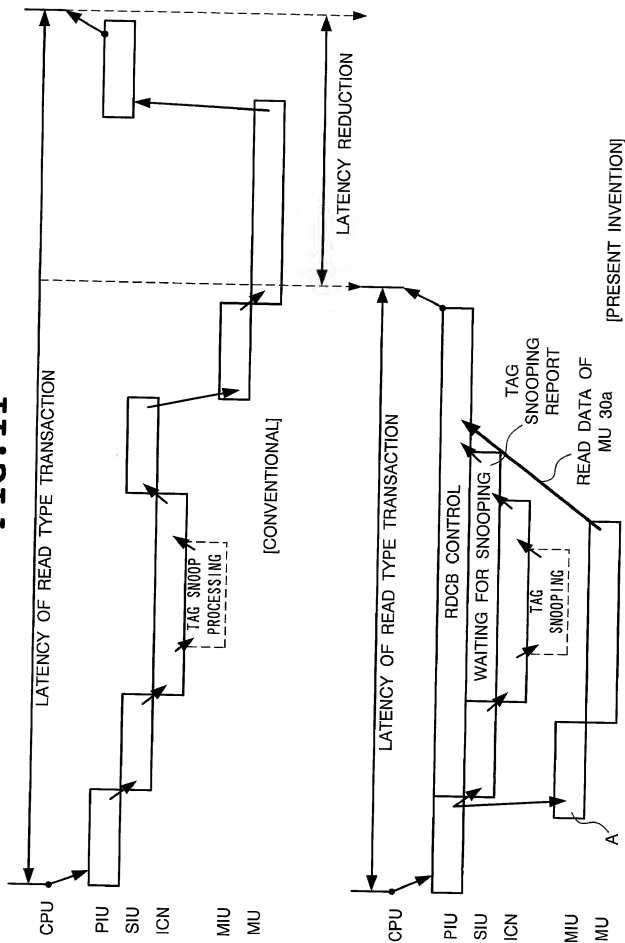
**FIG. 8**

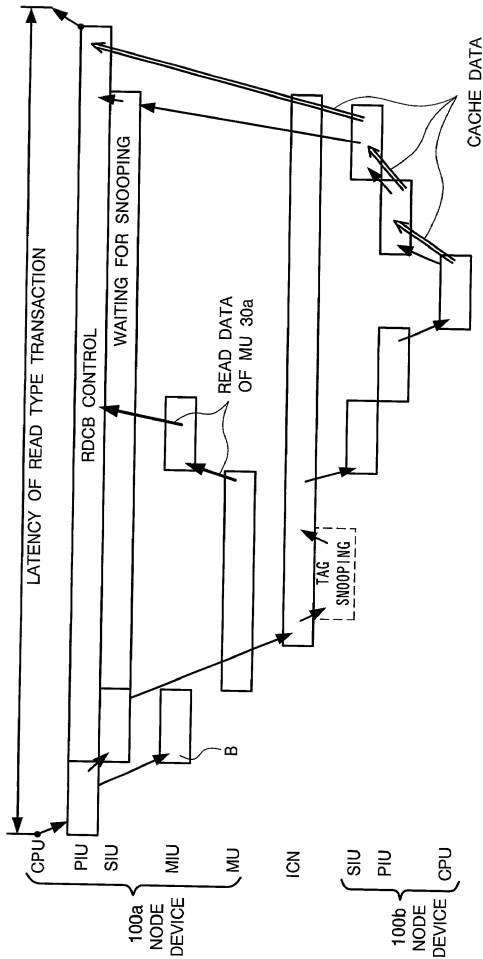
**FIG. 9**

V	BIT SHOWING THAT THE PROCESSOR HAS ISSUED A READ TYPE TRANSACTION AND IS WAITING FOR SNOOP PROCESSING
SNP	INFORMATION SHOWING THE SNOOP RESULT OBTAINED FROM THE INTERNAL CONNECTION NETWORK

**FIG. 10**

CASE	LV	TV	HV	CV	JV	PROCESSING CONTENTS
(1)	1	1	0	0	MODIFY NOT FOUND	LOCAL MEMORY DATA IS SENT TO THE PROCESSOR
(2)	1	1	0	1	MODIFY FOUND	CACHE DATA IS SENT TO THE PROCESSOR AND THE LOCAL MEMORY DATA (SPECULATIVE READOUT DATA) IS ABOLISHED
(3)	0	1	1	0	MODIFY NOT FOUND	MEMORY DATA IN THE REMOTE NODE IS SENT TO THE PROCESSOR
(4)	0	1	1	1	MODIFY FOUND	CACHE DATA IS SENT TO THE PROCESSOR AND THE MEMORY DATA IN THE REMOTE NODE IS ABOLISHED

**FIG. 11**

**FIG. 12**



The diagram illustrates the timing of a read type transaction between two nodes, 100a and 100b. A vertical double-headed arrow on the left indicates the "LATENCY OF READ TYPE TRANSACTION".

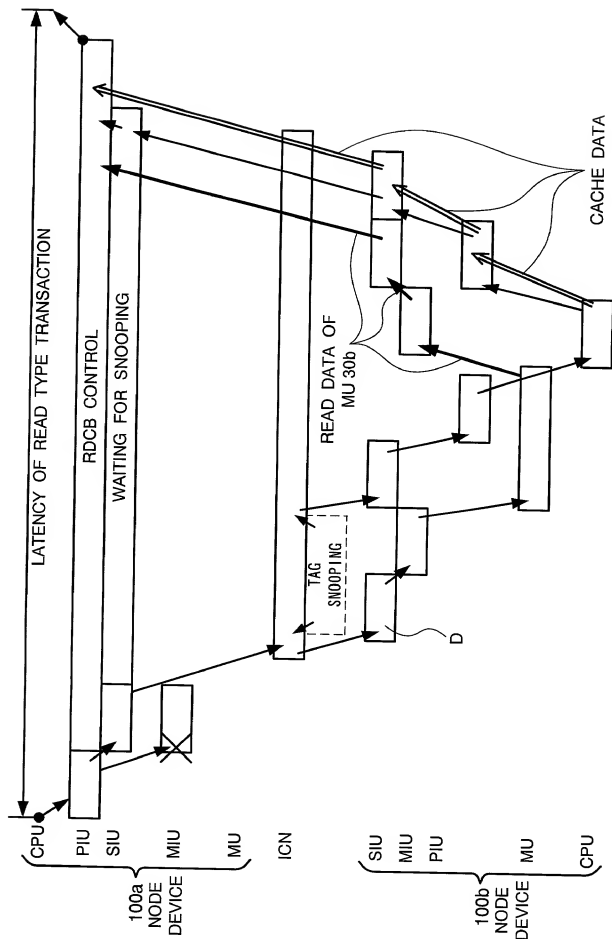
**Node 100a (Left):** Labeled "100a NODE DEVICE". It contains four components: CPU, PIU, SIU, and MIU. The MIU is marked with a large 'X'. The transaction flow is: CPU → PIU → SIU. The SIU has two states: "WAITING FOR SNOOPING" and "RDCB CONTROL".

**Node 100b (Right):** Labeled "100b NODE DEVICE". It contains three components: SIU, MIU, and MU. The SIU has a state "TAG SNOOPING" (indicated by a dashed box). The MU has a state "READ DATA OF MU 30b".

**ICU (Center):** A vertical bar representing the interconnect. Arrows show the signal path: from Node 100a SIU to ICU, and from ICU to Node 100b SIU and MU.

**Sequence of Events:**

- Node 100a CPU initiates the transaction.
- Node 100a PIU sends a signal to the ICU.
- Node 100a SIU enters "WAITING FOR SNOOPING".
- Node 100b SIU enters "TAG SNOOPING".
- Node 100b MU receives "READ DATA OF MU 30b".
- Node 100a SIU transitions to "RDCB CONTROL".

**FIG. 14**

**FIG. 15**

BLOCK NUMBER	STATUS INFORMATION	NODE DEVICE NUMBER
a	U	_____
⋮	⋮	⋮

**FIG. 16**

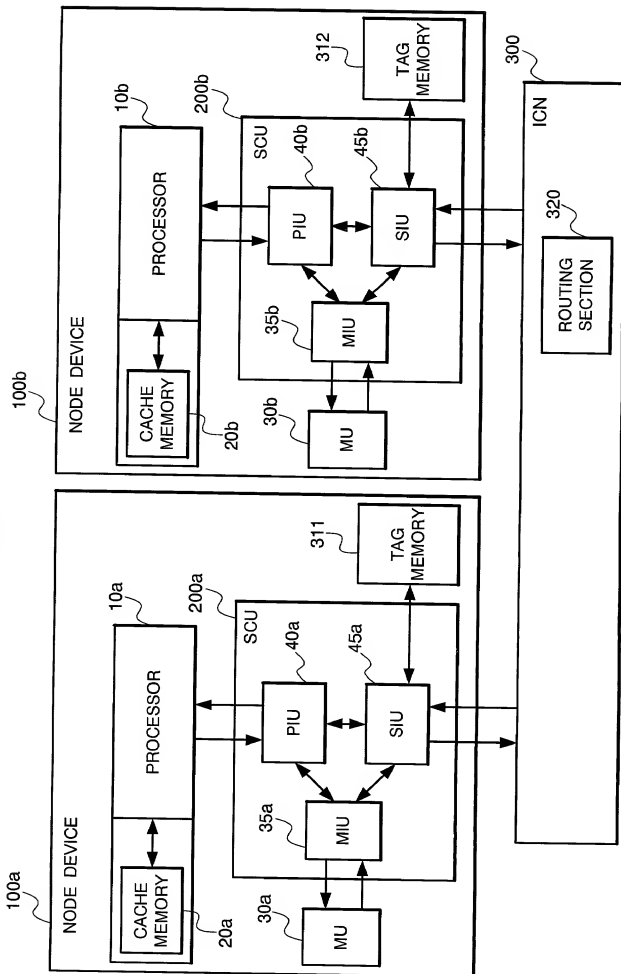
BLOCK NUMBER	STATUS INFORMATION	NODE DEVICE NUMBER
a	P	(2)
⋮	⋮	⋮

**FIG. 17**

BLOCK NUMBER	STATUS INFORMATION	NODE DEVICE NUMBER
b	U	_____
⋮	⋮	⋮

**FIG. 18**

BLOCK NUMBER	STATUS INFORMATION	NODE DEVICE NUMBER
b	P	(2)
⋮	⋮	⋮

**FIG. 19**

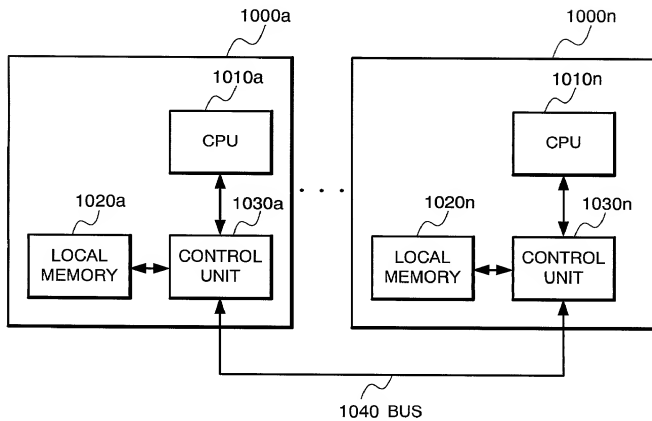
**FIG. 20**

(a)

V	SNP1	SNP2
1		

(b)

V	SNP1	SNP2
1	SNOOP RESULT	SNOOP RESULT

**FIG. 21** (PRIOR ART)

**FIG. 22** (PRIOR ART)